



UTKAL INSTITUTE OF ENGINEERING & TECHNOLOGY

| DISCIPLINE: Electrical Engineering | SEMESTER: 5thSem | NAME OF THE TEACHING FACULTY: ER. Chittaranjan Parida | | |
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| SUBJECT: | No of Days/ Per week class allotted: | Semester From Date:15/09/2022 To Date:22/12/2022 No. Of Weeks: 15 | | |
| DIGITAL ELECTRONICS & MICROPROCESSOR | 5 Class P/W | -75 | | |
| WEEK | CLASS DAY | THEORY TOPICS | REMARKS | |
| 1 st | 1 st | Binary, Octal, Hexadecimal number systems and compare | Date | Dean/Principal |
| | 2 nd | Binary addition, subtraction, Multiplication and Division | | |
| | 3 rd | 1's complement and 2's complement numbers for a binary number , Subtraction of binary numbers in 2's complement method. | | |
| | 4 th | Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa. | | |
| | 5 th | Doubt Clear Class | | |
| 2 nd | 1 st | Importance of parity Bit | | |
| | 2 nd | Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table. | | |
| | 3 rd | Realize AND, OR, NOT operations using NAND, NOR gates. | | |
| | 4 th | Different postulates and De-Morgan's theorems in Boolean algebra | | |
| | 5 th | Use Of Boolean Algebra For Simplification Of Logic Expression | | |
| 3 rd | 1 st | Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map. | | |
| | 2 nd | Give the concept of combinational logic circuits, Half adder circuit and verify its functionality using truth table. | | |

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| 5 | 3 rd | Realize a Half-adder using NAND gates only and NOR gates only | | |
| | 4 th | Full adder circuit and explain its operation with truth table. | | |
| | 5 th | Realize full-adder using two Half-adders and an OR – gate and write truth table | | |
| 4 th | 1 st | Full subtractor circuit and explain its operation with truth table | | |
| | 2 nd | Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer | | |
| | 3 rd | Working of Binary-Decimal Encoder & 3 X 8 Decoder. | | |
| | 4 th | Working of Two bit magnitude comparator. | | |
| | 5 th | Give the idea of Sequential logic circuits | | |
| 5 th | 1 st | State the necessity of clock and give the concept of level clocking and edge triggering, | | |
| | 2 nd | Clocked SR flip flop with preset and clear inputs | | |
| | 3 rd | Construct level clocked JK flip flop using S-R flip-flop and explain with truth table | | |
| | 4 th | Concept of race around condition and study of master slave JK flip flop. | | |
| | 5 th | Give the truth tables of edge triggered D and T flip flops and draw their symbols. | | |
| 6 th | 1 st | Applications of flip flops. | | |
| | 2 nd | Define modulus of a counter | | |
| | 3 rd | 4-bit asynchronous counter and its timing diagram | | |
| | 4 th | Assignment | | |
| | 5 th | Asynchronous decade counter. | | |
| 7 th | 1 st | 4-bit synchronous counter. | | |
| | 2 nd | Distinguish between synchronous and asynchronous counters. , State the need for a Register and list the four types of registers | | |
| | 3 rd | Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop. | | |
| | 4 th | Introduction to Microprocessors, Microcomputers | | |

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| | 5 th | Architecture of Intel 8085A Microprocessor and description of each block. | | |
| 8 th | 1 st | Pin diagram and description. | | |
| | 2 nd | Stack, Stack pointer & stack top | | |
| | 3 rd | Interrupts | | |
| | 4 th | Opcode & Operand | | |
| | 5 th | Differentiate between one byte, two byte & three byte instruction with example., Instruction set of 8085 example | | |
| 9 th | 1 st | Revision of last classes | | |
| | 2 nd | Assignment question Discussion | | |
| | 3 rd | Addressing mode | | |
| | 4 th | Fetch Cycle, Machine Cycle, Instruction Cycle, T-State | | |
| | 5 th | Timing Diagram for memory read, memory write, I/O read, I/O write | | |
| 10 th | 1 st | Class Test | | |
| | 2 nd | Internal Question Discussion | | |
| | 3 rd | Doubt Clear Class | | |
| | 4 th | Doubt Clear Class | | |
| | 5 th | Timing Diagram for 8085 instruction | | |
| 11 th | 1 st | Timing Diagram for 8085 instruction | | |
| | 2 nd | Revision | | |
| | 3 rd | Counter and time delay | | |
| | 4 th | Simple assembly language programming of 8085. | | |
| | 5 th | Simple assembly language programming of 8085. | | |
| 12 th | 1 st | Assignment | | |
| | 2 nd | Assignment question Discussion | | |
| | 3 rd | Class Test | | |
| | 4 th | Sample Paper Important Question Discussion | | |
| | 5 th | Basic Interfacing Concepts, Memory mapping & I/O mapping | | |
| | 1 st | Revision of last class | | |
| | 2 nd | Timing Diagram for 8085 instruction | | |

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| 13 th | 3 rd | Assignment | | |
| | 4 th | Counter and time delay. | | |
| | 5 th | Assignment question Discussion | | |
| 14 th | 1 st | Simple assembly language programming of 8085. | | |
| | 2 nd | Simple assembly language programming of 8085. | | |
| | 3 rd | Basic Interfacing Concepts, Memory mapping & I/O mapping | | |
| | 4 th | Functional block diagram and description of each block of Programmable peripheral interface Intel 8255 , | | |
| | 5 th | Class Test | | |
| 15 th | 1 st | Class Test | | |
| | 2 nd | Revision | | |
| | 3 rd | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller | | |
| | 4 th | Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller | | |
| | 5 th | Important questions will be discussed for the semester Exam. | | |

Chittaranjan Tarida

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Chittaranjan Tarida

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PRINCIPAL